

## Automotive-grade N-channel 600 V, 5 A, 0.84 $\Omega$ typ., MDmesh™ II Power MOSFETs in D<sup>2</sup>PAK and DPAK packages

Datasheet - production data

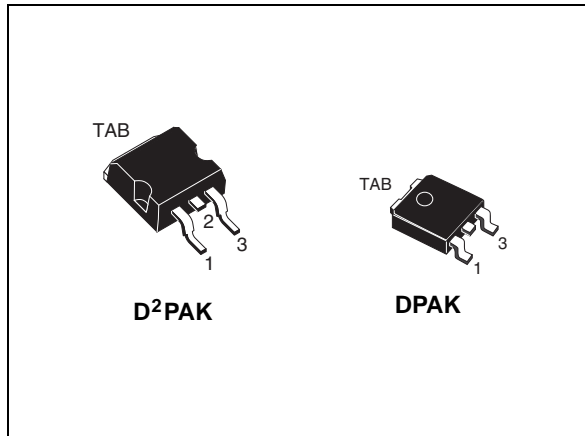
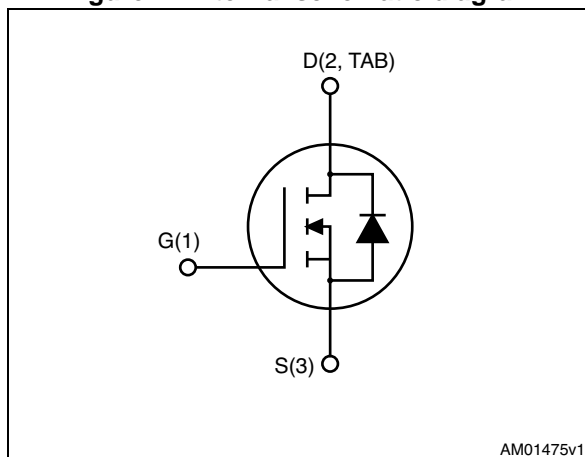


Figure 1. Internal schematic diagram



### Features

Order codes	$V_{DS}$ @ $T_{jmax}$	$R_{DS(on)}$ max.	$I_D$
STB7ANM60N	650 V	0.9 $\Omega$	5 A
STD7ANM60N			

- Designed for automotive applications and AEC-Q101 qualified
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET associates a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Packages	Packaging
STB7ANM60N	7ANM60N	D <sup>2</sup> PAK	Tape and reel
STD7ANM60N		DPAK	

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ ,  $V_{DS(Peak)} < V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value		Unit
		D <sup>2</sup> PAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max	2.78		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	35	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch<sup>2</sup> FR-4 board, 2oz Cu

**Table 4. Thermal data**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	119	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 600\text{ V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 2.5\text{ A}$		0.84	0.9	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	363	-	pF
$C_{oss}$	Output capacitance		-	24.6	-	pF
$C_{rss}$	Reverse transfer capacitance		-	1.1	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Output equivalent capacitance	$V_{DS} = 0\text{ to }480\text{ V}$ , $V_{GS} = 0$	-	130	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 5\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 16</a> )	-	14	-	nC
$Q_{gs}$	Gate-source charge		-	2.7	-	nC
$Q_{gd}$	Gate-drain charge		-	7.7	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$ .

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 2.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 17</a> )	-	7	-	ns
$t_r$	Rise time		-	10	-	ns
$t_{d(off)}$	Turn-off-delay time		-	26	-	ns
$t_f$	Fall time		-	12	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5 \text{ A}$ , $V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 20</a> )	-	213		ns
$Q_{rr}$	Reverse recovery charge		-	1.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	14		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 20</a> )	-	265		ns
$Q_{rr}$	Reverse recovery charge		-	1.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	14		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for D<sup>2</sup>PAK

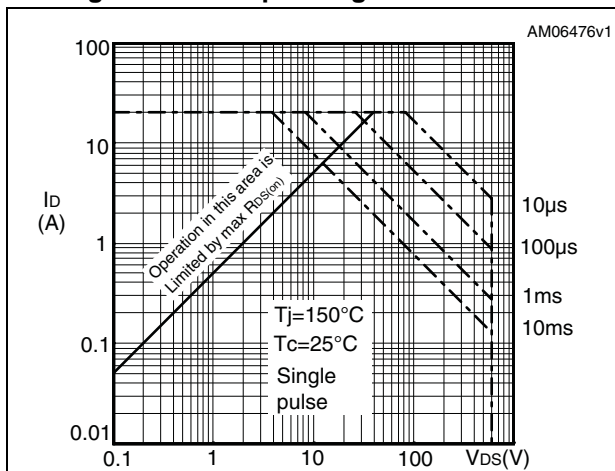


Figure 3. Thermal impedance for D<sup>2</sup>PAK

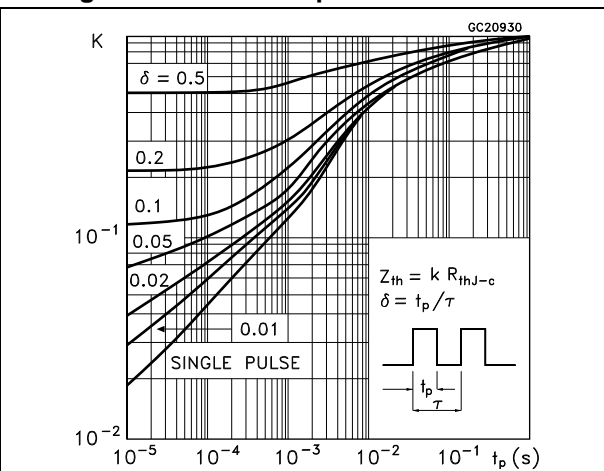


Figure 4. Safe operating area for DPAK

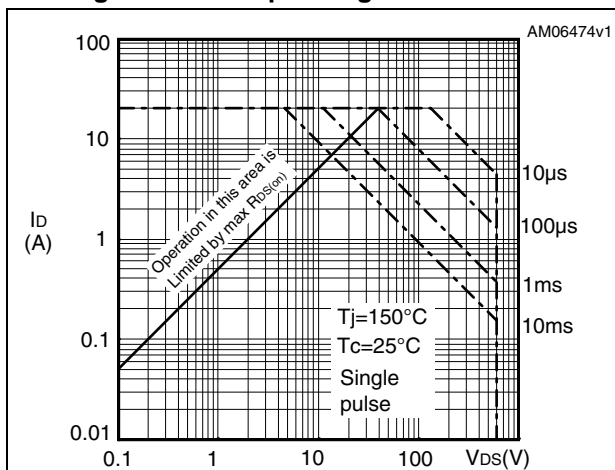


Figure 5. Thermal impedance for DPAK

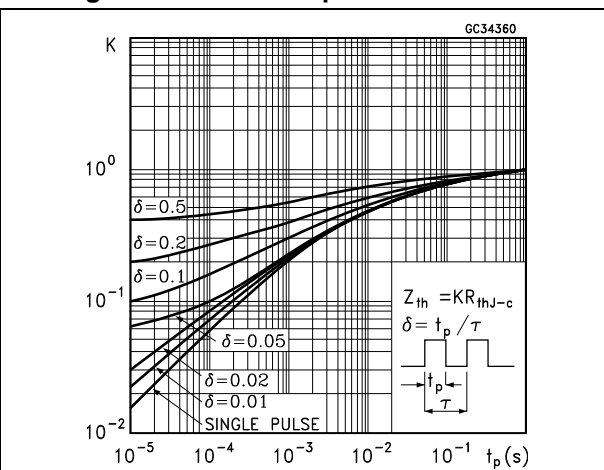


Figure 6. Output characteristics

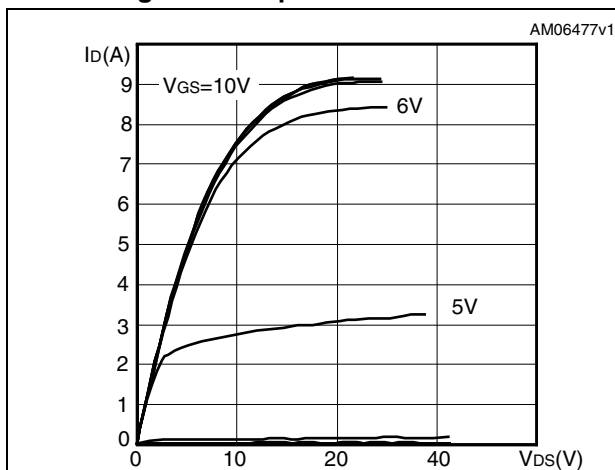


Figure 7. Transfer characteristics

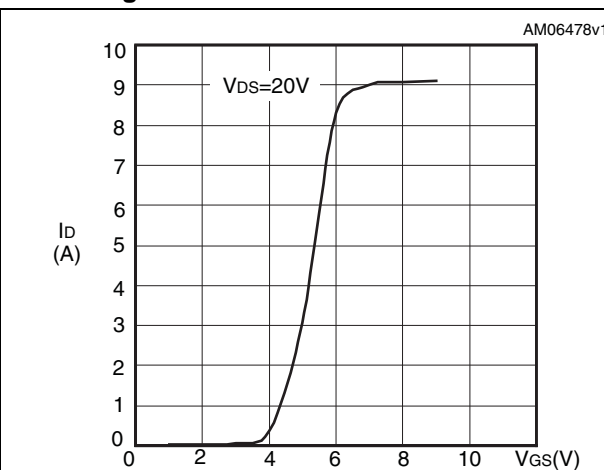


Figure 8. Gate charge vs gate-source voltage

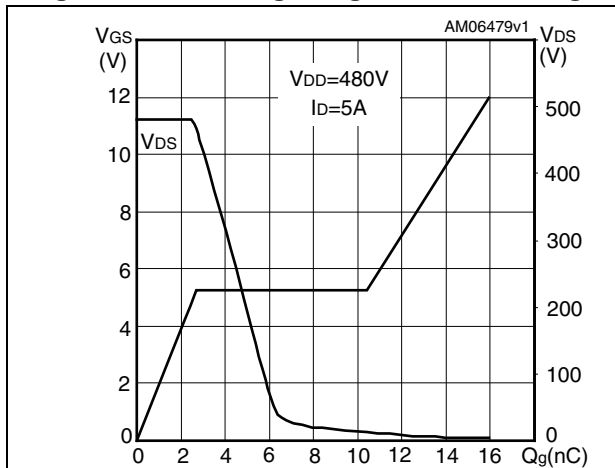


Figure 9. Static drain-source on resistance

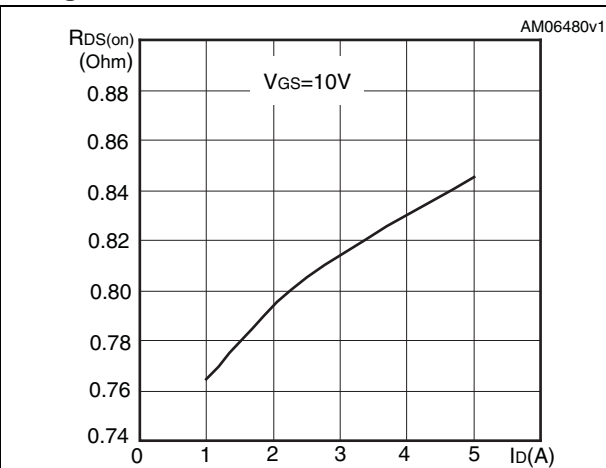


Figure 10. Capacitance variations

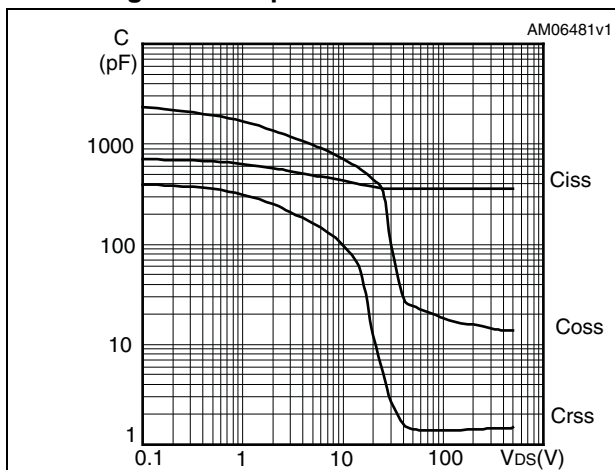


Figure 11. Output capacitance stored energy

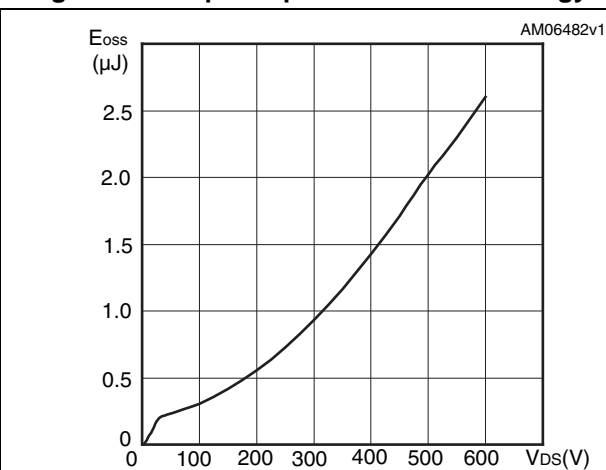


Figure 12. Normalized gate threshold voltage vs temperature

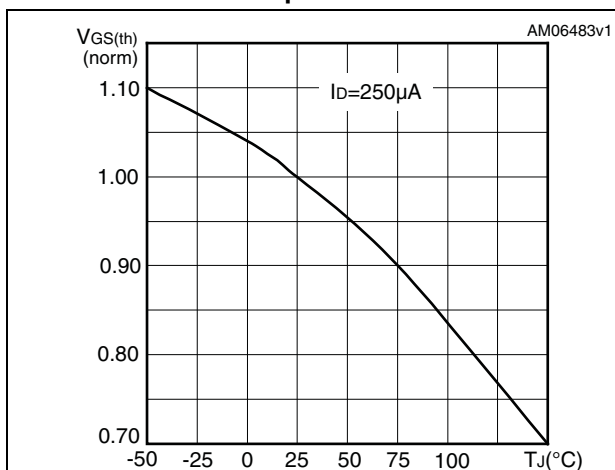


Figure 13. Normalized on-resistance vs temperature

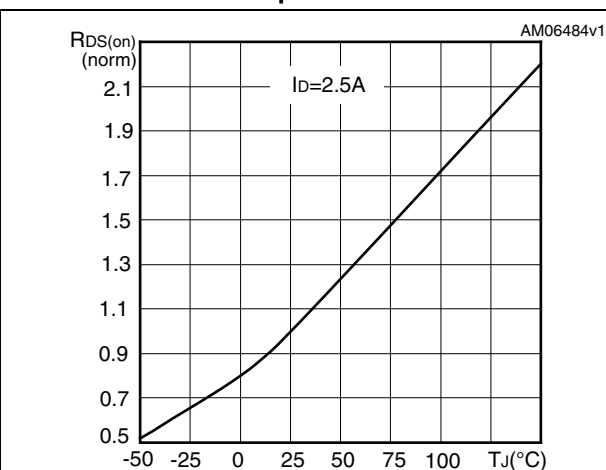
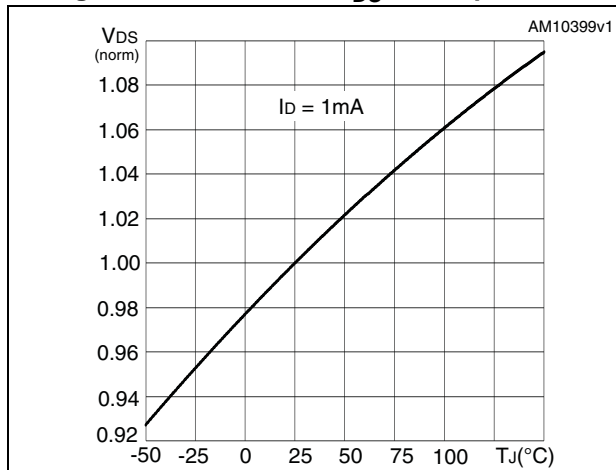


Figure 14. Normalized  $V_{DS}$  vs temperature





### 3 Test circuits

Figure 15. Switching times test circuit for resistive load



Figure 16. Gate charge test circuit

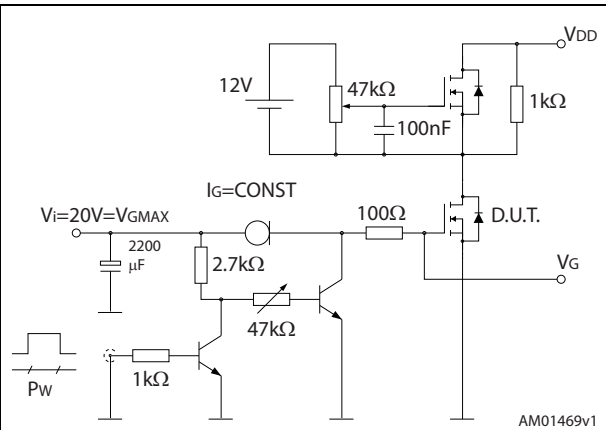


Figure 17. Test circuit for inductive load switching and diode recovery times

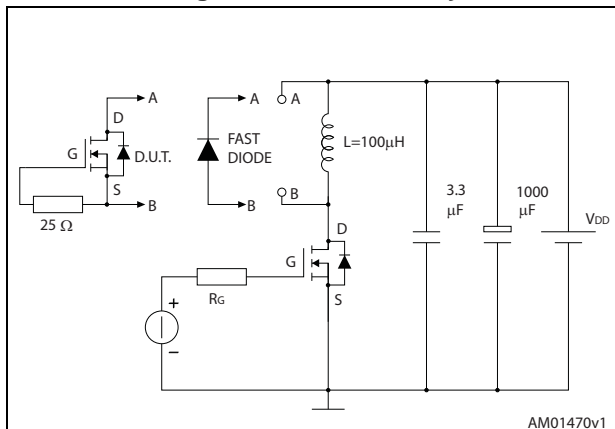


Figure 18. Unclamped inductive load test circuit

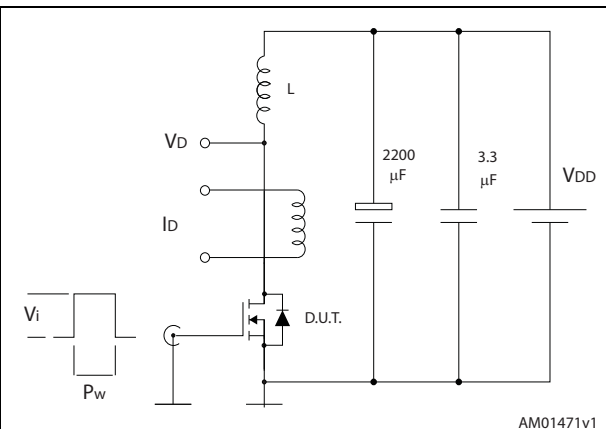


Figure 19. Unclamped inductive waveform

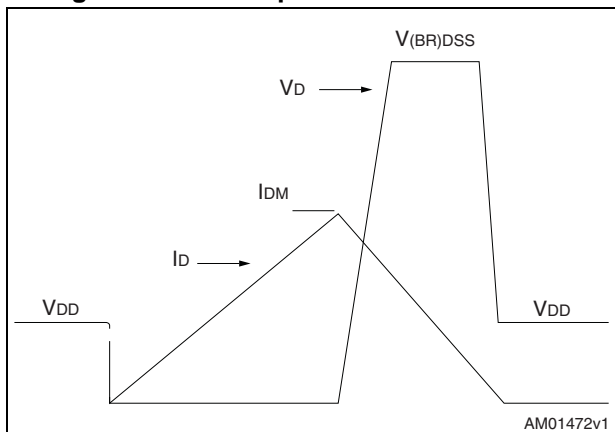
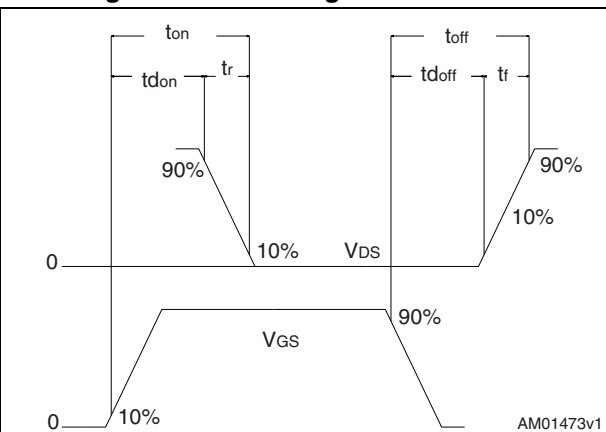


Figure 20. Switching time waveform



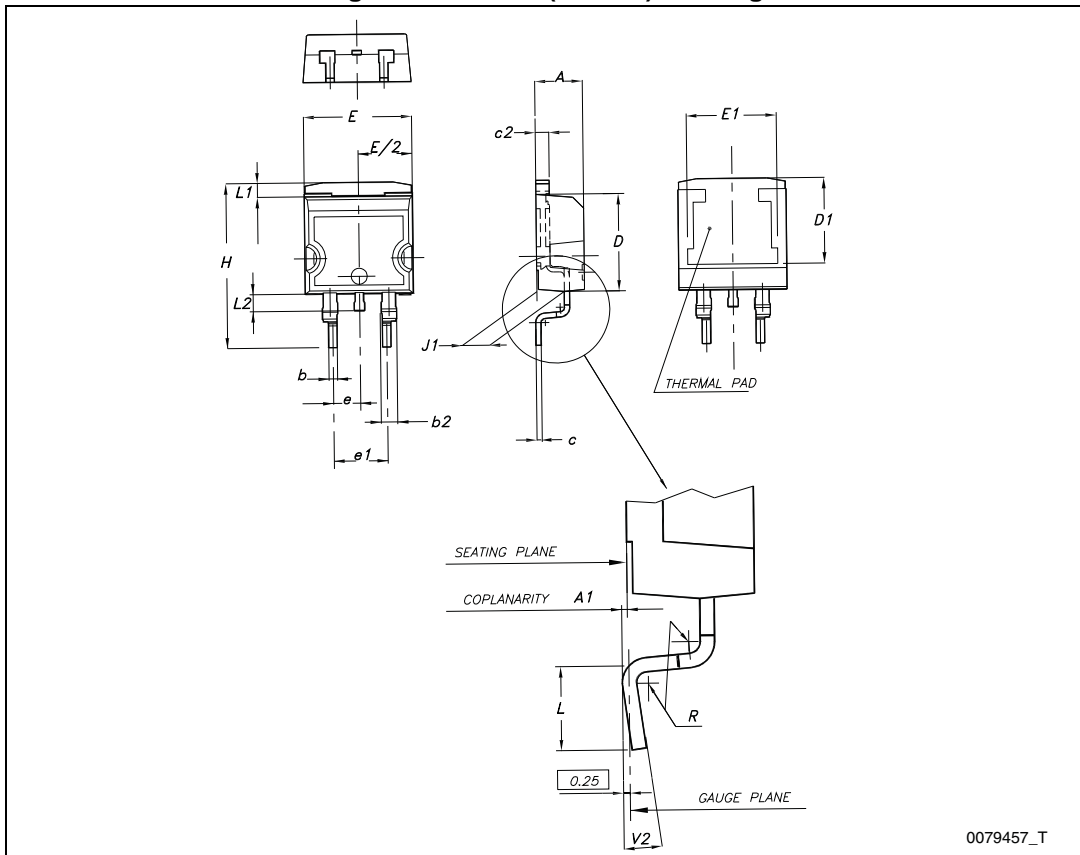
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Table 9. D<sup>2</sup>PAK (TO-263) mechanical data

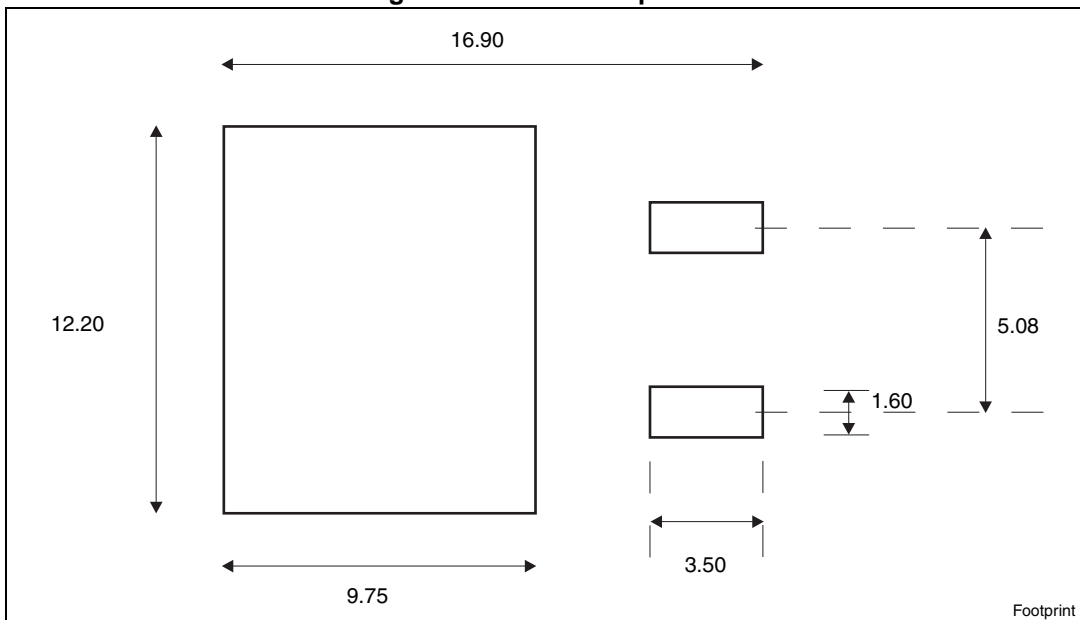
Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50		
E	10		10.40
E1	8.50		
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 21. D<sup>2</sup>PAK (TO-263) drawing



0079457\_T

Figure 22. D<sup>2</sup>PAK footprint<sup>(a)</sup>



Footprint

a. All dimensions are in millimeters

Table 10. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)		2.80	
L2		0.80	
L4	0.60		1.00
R		0.20	
V2	0°		8°

Figure 23. DPAK (TO-252) type A drawing

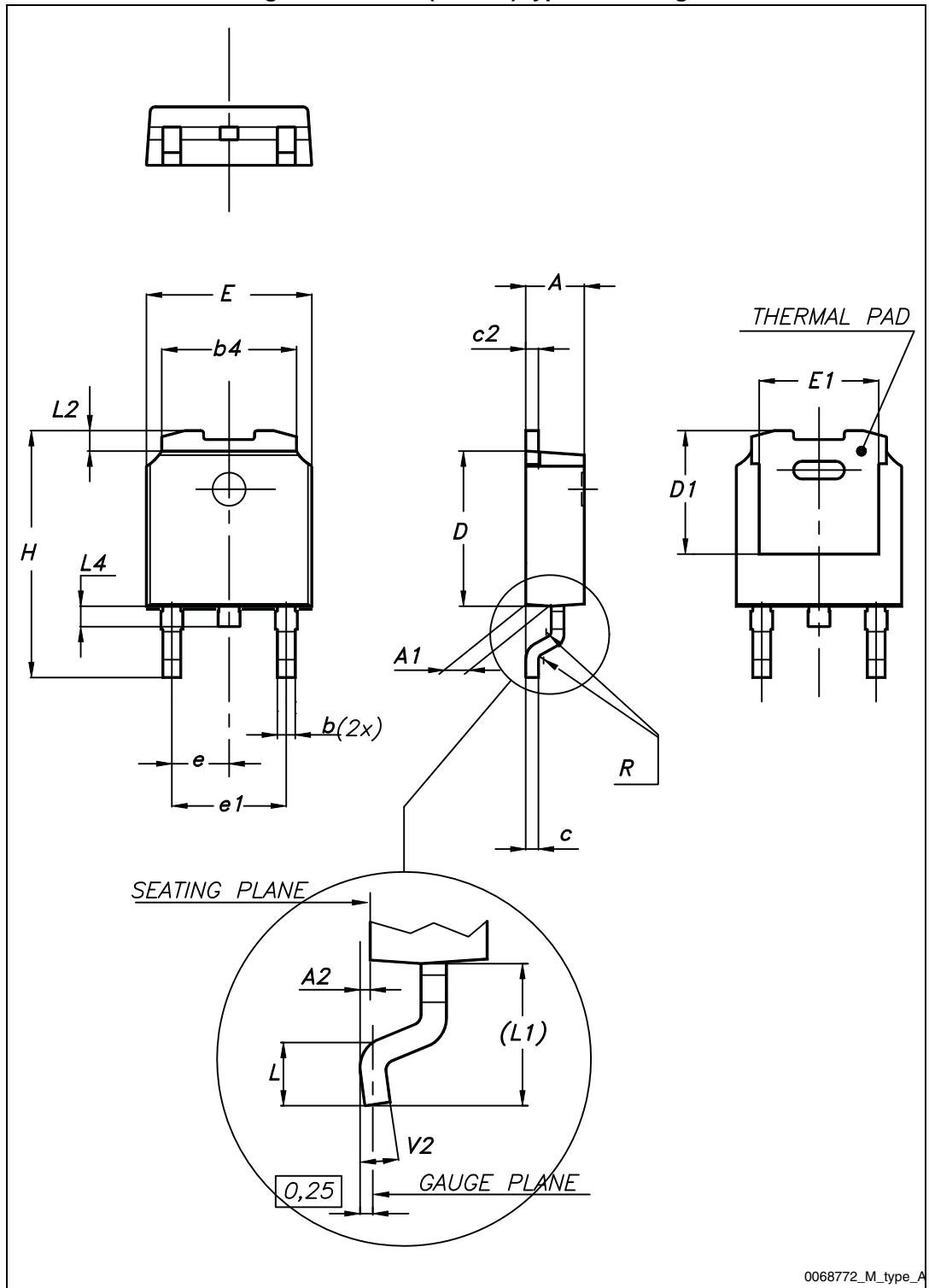
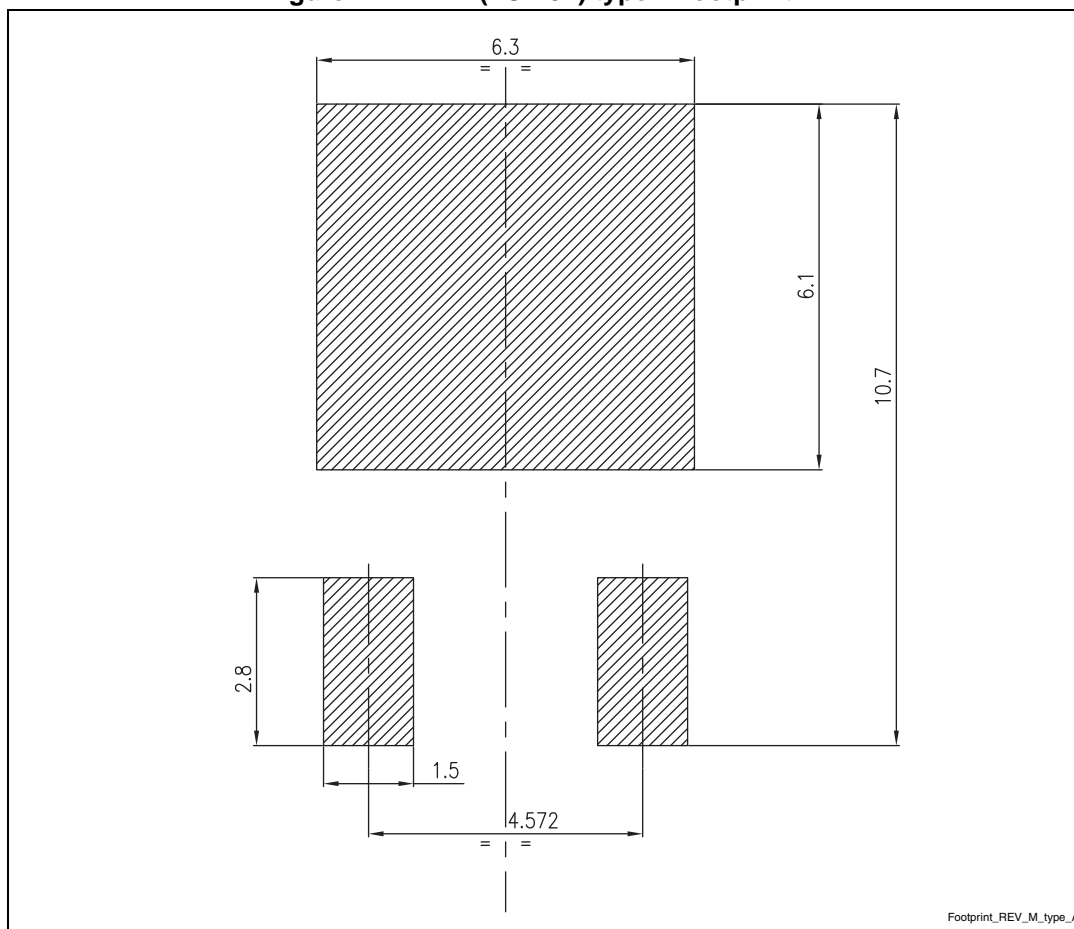


Figure 24. DPAK (TO-252) type A footprint (b)



b. All dimensions are in millimeters

## 5 Packaging mechanical data

Table 11. D<sup>2</sup>PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1		Base qty.	2500
P1	7.9	8.1		Bulk qty.	2500



Table 12. DPAK (TO-252) tape and reel mechanical data (continued)

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 25. Tape

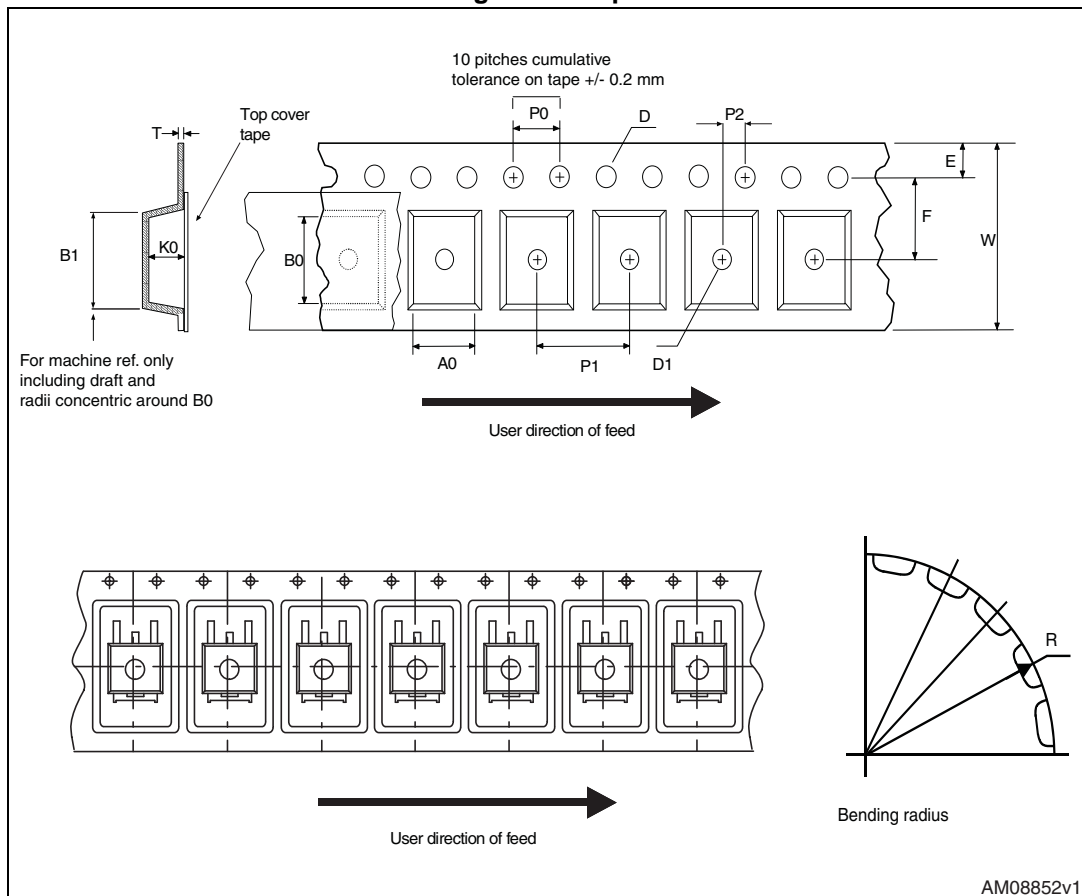
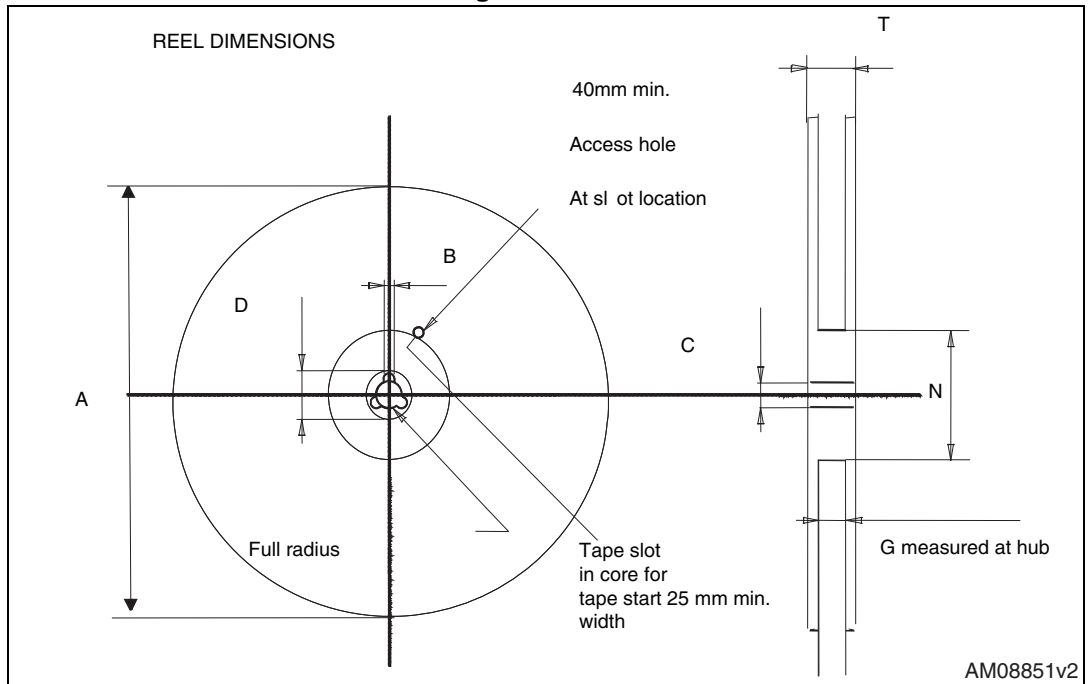


Figure 26. Reel



## 6 Revision history

Table 13. Document revision history

Date	Revision	Changes
21-Jun-2012	1	First issue.
12-Dec-2013	2	<ul style="list-style-type: none"><li>– Modified: title, <i>Features</i> and <i>Table 1</i> in cover page</li><li>– Modified: <i>Figure 15, 16, 17</i> and <i>18</i></li><li>– Updated: <i>Table 10</i> and <i>Figure 23, 24</i></li><li>– Minor text changes</li></ul>

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